Express label: EL046036854US

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920010149US1	10/064,486
Applicant(s)	
Ditlow et al.	
Filing Date	**Group Art Unit**
07/19/2002	Unknown

PATENT & TRADEMARK OFFICE JUL 30 2002 OPE JC43

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
T.P.		5754829	5/19/98	Motohiro et al.	709	201	
T.P.		5928328	7/27/99	Komori et al.	709	223	
T.P.		5708832	1/13/98	Inniss et al.	709	229	
T.P.		5845627	12/8/98	Olin et al.	123	621	676
T.P.		5930773	7/27/99	Crooks et al.	705	30	

RECEIVED
AUG 05 2002
Technology Center 2100

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

T.P.		Dooling et al., "Parallel Domain Decomposition for Integrated Circuit Designs." Presented at the First SIRM Conference on Computational Science and Engineering, September 21, 2000, Washington, D.C.

EXAMINER	Thai Phan	DATE CONSIDERED	8/5/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.